CLAIMS

What is Claimed is:

1. A semiconductor device comprising:

a pad metal layer having a perimeter area and a center area;

a lower metal layer having a plurality of apertures below said center area of said pad metal layer; and

an interlayer dielectric formed between said pad metal layer and said lower metal layer.

2. The semiconductor device as recited in Claim 1 further comprising:

a plurality of vias formed in said interlayer dielectric, wherein said vias electrically couple said pad metal layer and said lower metal layer, and wherein said vias are located below said perimeter area of said pad metal layer.

3. The semiconductor device as recited in Claim 2 wherein said vias are filled with tungsten.

4. The semiconductor device as recited in Claim 2 wherein said vias are positioned in a ring arrangement below said pad metal layer.

5. The semiconductor device as recited in Claim 2 further comprising an insulating dielectric layer that covers said perimeter area of said pad metal layer.

6. The semiconductor device as recited in Claim 1 wherein a probing process is performed on said center area of said pad metal layer.

7. The semiconductor device as recited in Claim 1 wherein a wire-bonding process is performed on said center area of said pad metal layer.

8. The semiconductor device as recited in Claim 1 wherein said semiconductor device is an integrated circuit chip.

9. A semiconductor device comprising:

a pad metal layer having a perimeter area and a center area;

a lower metal layer having a plurality of apertures below said center area of said pad metal layer;

an interlayer dielectric formed between said pad metal layer and said lower metal layer; and

a plurality of vias formed in said interlayer dielectric, wherein said vias electrically couple said pad metal layer and said lower metal layer, and wherein said vias are located below said perimeter area of said pad metal layer.

10. The semiconductor device as recited in Claim 9 wherein said vias are filled with tungsten.

11. The semiconductor device as recited in Claim 9 wherein said vias are positioned in a ring arrangement below said pad metal layer.

12. The semiconductor device as recited in Claim 9 further comprising an insulating dielectric layer that covers said perimeter area of said pad metal layer.

13. The semiconductor device as recited in Claim 9 wherein a probing process is performed on said center area of said pad metal layer.

14. The semiconductor device as recited in Claim 9 wherein a wire-bonding process is performed on said center area of said pad metal layer.

15. The semiconductor device as recited in Claim 9 wherein said semiconductor device is an integrated circuit chip.

16. A method of electrically coupling a pad metal layer and a lower metal layer in a semiconductor device, said method comprising:

forming a plurality of apertures in said lower metal layer, wherein said pad metal layer has a perimeter area and a center area, and wherein said apertures are located below said center area of said pad metal layer;

forming a plurality of vias in a interlayer dielectric between said pad metal layer and said lower metal layer, and wherein said vias are located below said perimeter area of said pad metal layer; and

filling said vias with a metal.

17. The method as recited in Claim 16 wherein said metal is tungsten.

18. The method as recited in Claim 16 wherein said vias are positioned in a ring arrangement below said pad metal layer.

19. The method as recited in Claim 16 further comprising forming an insulating dielectric layer that covers said perimeter area of said pad metal layer.

20. The method as recited in Claim 16 further comprising performing a probing process on said center area of said pad metal layer.

21. The method as recited in Claim 16 further comprising performing a wire-bonding process on said center area of said pad metal layer.

22. The method as recited in Claim 16 wherein said semiconductor device is an integrated circuit chip.